The Origin and Suppression of Limit Cycles in Digitally Controlled RF PA Loops

Patrick Pratt
Motorola Ireland Design Centre, Building 3400, Airport Business Park, Cork, Ireland
Tel: +353 (0)21 4910200, Fax: +353 (0)21 4910201
email: patrick.pratt@motorola.com

Abstract — **The origin of limit cycles in digitally controlled RF PA loops is analysed using the theory of Describing Functions and is shown to result from a code dependent gain caused by DAC quantisation. The effects of the limit cycle in terms of spec compliance for the particular case of the GSM protocol are examined. It is shown how compliance can be maintained even in the presence of limit cycles by carefully specifying the control slope of the PA. Finally, in the case where the PA control slope cannot be constrained, it is shown how the introduction of an intentional nonlinearity into the loop can be exploited to suppress the limit cycle.**

I. INTRODUCTION

In TDMA systems the switching constraints on the RF output pulse transmission are rigorously defined. In the case of the GSM system these constraints are dictated by the ESTI spec 05.05 and 11.10 [1] in terms of a power versus time template, and a spectrum mask for both the full pulse and modulation only phase. Although an open loop control strategic can be adopted to switch the PA, a closed loop approach is invariably required to provide the necessary degree of insensitivity to PA characteristic variation. In order to capitalise on the evolution towards an all-digital CMOS process and facilitate the requirement for multimode phones a digital realisation of the loop is obvious. Motorola now offers a full GSM/GPRS mixed signal transceiver chip set solution, [2] that contains such a Power Amplifier Control (PAC) loop as a subsystem.

A simplified block diagram of the loop is illustrated in fig. 1.

The PA, coupler and detector, in addition to the RF switches for the GSM900, DCS1800 and PCS1900 bands are contained in the module, MMM6010, [6]. The detector voltage is feedback to the baseband processor IC, the DSP56621 [2], where it is filtered and digitised by a 10b two-step, 2.6Msps converter. The detected digital code is then subtracted from the desired power-reference waveform to produce the control error. The control algorithm consists of a two-term controller, adaptive bandwidth and saturation detection and correction mechanisms. The 22b control output word is then truncated to 10b, applied to a 10b thermometer-code, current DAC, filtered and then buffered to produce the bias voltage for the PA.

The transceiver, which is targeted at the merchant market, is currently available on a CMOS 0.13 µm process and is currently featuring in the recently announced i.250 platform of Motorola phones [3]

The following paper describes, using the theory of Describing Functions how the quantisation nonlinearity presence in the DAC gives rise to limit cycles and possible spec incompliance. Guidelines on the selection of a suitable PA that ensures spec compliance are provided. In the particular case where these PA constraints cannot be satisfied a novel technique to suppress unwanted limit cycles is presented.

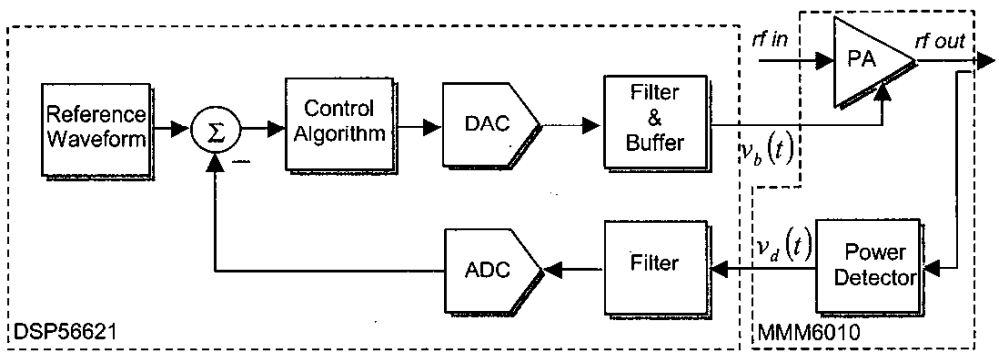

Fig. 1 Simplified Block Diagram of a i.250 Digitally Controlled RF PA Loop

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II. DESCRIBING FUNCTION ANALYSIS

The quantisation effect of a data converter is conventionally and conveniently often modelled as additive white noise [4]. For constant amplitude modulation schemes, such as GSM, during the modulation phase the DAC input code will be insufficiently rich in spectral content to justify the assumptions underlying this model. Instead, a nonlinear as opposed to stochastic approach must be taken. For instance, consider the case where an ideal 10b DAC is stimulated by a pure tone of amplitude ½b. The quantised output will be a square wave of amplitude 1b. Those for a pure tone input the output will consist of a fundamental and odd harmonics; a classic indication of nonlinear behaviour.

Typical of most digital control loops, if a reconstruction filter possessing a cut off frequency sufficiently low enough to attenuate the harmonics to a negligible level follows the DAC, then a quasi-linear analysis may be adopted. Under this assumption only the gain of the fundamental output relative to the input tone need be considered. However, the remarkable and fundamental features of this gain, (or Describing function as it is referred to in the control literature [5]), is that it is not constant but depends on the input code changes. Illustrated in fig. 2 is the code dependent gain for an ideal 10b DAC. Observe that as the code changes exceed 1b the effective gain tends to unity. Conversely, as the code changes become infinitesimally small the gain tends to infinity.

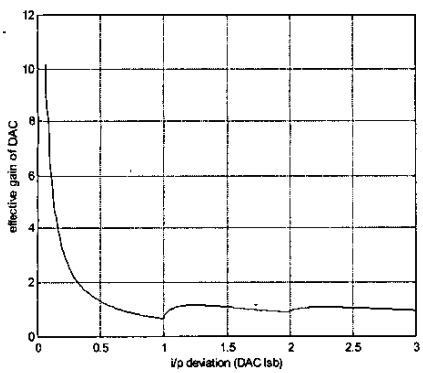

Fig. 2 Describing Function for 10 bit DAC

During the modulation phase the output power must be regulated within a well-defined limit. For instance, the GSM ESTI spec 05.05 [1] dictates that the power must be controlled to within ±1dB. The controller must then be designed such that the PA bias voltage and hence the DAC input code changes tend towards zero. Based on the above analysis, if the code changes diminish, the gain presented by the DAC will increase towards infinity. Assuming sufficient lag throughout the loop this increasing DAC gain would eventually result in instability. However, the onset of instability is accompanied by growing transients and hence larger code changes and thus a reduction in gain. In effect, the loop can only behave in a marginally stable manner, as neither stable nor unstable behaviour is possible. In a linear sense, the code dependent gain of the DAC converges towards the 'Ultimate Gain', which makes the loop marginally stable. In the limit the behaviour of the loop becomes periodic or cyclic and is immediately recognised as a limit cycle. Fig. 3.1 illustrates an example of a limit cycle with respect to the power-time mask and fig. 3.2 the corresponding modulation Output Radio frequency Spectrum (ORFS) [1]. The AM component of the limit cycle introduces a spur that mixes with the baseband signal, which depending on its offset and magnitude can compromise manufacturing margins and ultimately failure of the modulation ORFS specification.

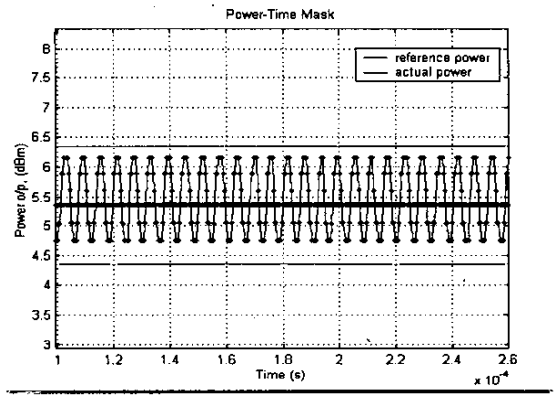

Fig. 3.1 Power-Time

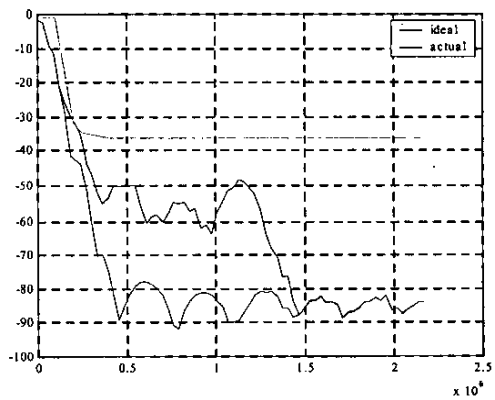

Fig. 3.2 Modulation ORFS

A more classical and rigorous explanation for this behaviour is available in the form of the extended Nyquist stability criterion [5] where the describing function becomes a locus of critical points as opposed to one critical point at $s=-1$ that is characteristic of linear systems. For the case of the DAC the describing functions traces a locus along the negative real axis in the s-plane. The locus of the remaining loop dynamics, provided there is sufficient phase lag, will intersect the describing function locus and hence satisfy the conditions for a limit cycle.

III. ETSI Compliance & PAC Limit Cycles

The presence of a DAC induced limit cycle need not necessarily imply compliance failure. In practice a limit cycle can be presence but with sufficiently low enough amplitude that both the power-time and modulation ORFS requirements can still be satisfied. Ultimately, it is the amplitude of the limit cycle at the PA output that determines whether the limit cycle will be problematic or not.

The amplitude of the cycle at the DAC output, according to the Describing Function analysis, is 1b. The amplitude of the limit cycle at the PA output then depends on the gain between the DAC and the PA output. Given that there is a fixed gain between the PA output and the detector output the limit cycle amplitude can also be expressed in terms of the PA 'control gain' between the PA input bias and detector output voltages, $\frac{\Delta v_d}{\Delta v_b} = G_{PA}$.

By carefully constraining this gain it is possible to control the amplitude of the limit cycle at the PA output and avoid compliance failure. For a given loop configuration it is possible to determine the upper range for the limit cycle amplitude before the modulation ORFS and the power-time requirements are violated. This limit can then be translated into a control gain constraint. Note the modulation ORFS and the power-time requirements are a function of output power so that this constraint has to be evaluated overall intended power levels. It will also be necessary to examine the control gain across frequency, input power, supply and temperature to determine the worst-case scenario. Fig. 4 illustrates the gain constraint derived for both the modulation ORFS and power-time requirements compared to a nominal control slope for the MMM6010, (the RF PA subsystem of the i.250 chip set solution [6]), for the GSM900 band at room temperature.

IV. Limit Cycle Suppressor

In the situation where the PA gain cannot be constrained to be within the above limit then remedial action will be required. One proposal is to introduce an intentional nonlinearity into the loop, which has a code dependent gain that is the inverse of the DAC's (patent pending [7]). The objective being that the gains effectively neutralises or cancels each other resulting in a constant or code independent gain. Although attractive in principle, the implementation of such a nonlinearity would prove costly. In practice is it sufficient to neutralize the large gain effect only for 'small' changes in the DAC input code. This can be readily achieved, for example, by a nonlinearity such as a deadzone described by

$$e_N(n)=\begin{cases}0 & |e(n)|\le\delta\\ e(n) & |e(n)|>\delta\end{cases}$$

where δ is the span of the deadzone. In essence the deadzone nonlinearity combines with the DAC quantisation nonlinearity to give a composite code dependent gain throughout the loop. In particular, δ is chosen to realise the desired amplitude dependent gain for diminishing code changes. Fig. 5 illustrates the Describing Function for a deadzone nonlinearity combined with the nonlinearity of a 10b DAC. Here the deadzone was applied to the error signal and spanned 1b. The essential feature is the diminishing gain as the input code changes tend to zero. As the loop settles and the controller code changes tend to zero, the combined gain also tends to zero removing the root cause for a limit cycle and hence allowing the loop to settle into non-cyclic steady state behaviour.

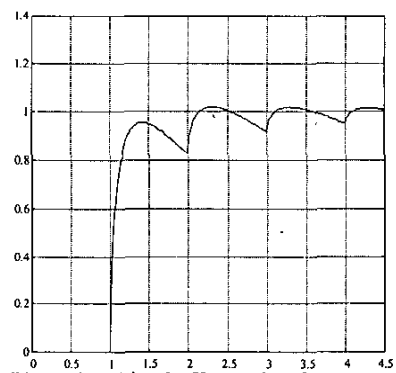

Fig. 5 Combined effect gain of an error deadzone and a DAC

V. CONCLUSION

In TDMA based protocols such as GSM the power profile of the RF output burst is strictly prescribed. When a digital closed loop control system is employed to obtain the necessary degree of power regulation, limit cycles due to DAC quantisation nonlinearity can occur. It was shown, using the theory of Describing Functions, how this nonlinearity can be modelled as a code dependent gain that tends towards infinity as the DAC input code changes reduce. It was further shown how this inverse gain effect gives rise to limit cycle behaviour.

For the particular case of GSM such limit cycles can cause power-time and modulation ORFS failure. By carefully constraining the gain between the PA input bias voltage and the detector output voltage it was shown how these problems can be avoided. In the case where the gain cannot be constrained a novel technique for suppressing limit cycles was introduced. An additional nonlinearity was intentionally introduced into the loop to neutralized the inverse gain effect of the DAC near small code changes and hence eliminate the limit cycles.

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